

ABSTRACT OF THE DISCLOSURE

A field-programmable gate array device (FPGA) having plural rows and columns of logic function units (VGB's) further includes a plurality of embedded memory blocks, where each memory block is embedded in a corresponding row of logic function units. Each embedded memory block has a registered address port for capturing received address signals in response to further-received, address-validating clock signals. Interconnect resources are provided for conveying the address-validating clock signals to address-changing circuitry so that a next address can be generated safely in conjunction with the capturing by the registered address port of a previous address signal.